

Faculty of Engineering - Port Said University Volume 29 No. 1 pp: 92:101



Output Voltage Harmonics Mitigation in Static Frequency Converter for Shore to Ship Power Connection Supplying Nonlinear Loads using Multi-frequency Quasi Resonant Controller

Mahmoud Fawzi^{1*}, Mahmoud Elghonimy², Ahmed E. Kalas¹, Gamal Abdel Azeem¹

¹ Electrical Engineering Department, Faculty of Engineering, Port Said University, Port Said, Egypt, email: <u>mah_fawzi@eng.psu.edu.eg</u> ² Electrical Engineering Dept., Port said Shipyard, Suez Canal Authority, Port Said, Egypt, email: <u>elghonimy89@gmail.com</u>, *Corresponding author, DOI: 10.21608/PSERJ.2024.309879.1359

ABSTRACT

Received 12-8-2024 Revised 2-9-2024 Accepted 16-9-2024

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Static frequency converter (SFC) is considered one of the main parts of the shore to ship power connection to match the frequency between the utility grid and ships docked at berth. Onboard nonlinear loads such as diode rectifiers and LED lamps distort the SFC output voltages with 3rd, 5th and 7th harmonics. Passive and active filters are usually used to mitigate these harmonics which increase the overall size and cost and reduce the system reliability. This paper proposes a multi-frequency quasi resonant harmonic compensator (MFQR-HC) for compensating these harmonics. The SFC mathematical model is presented, and the corresponding transfer functions are obtained. The proposed control system is designed in the stationary reference frame and analyzed in frequency domain considering reference tracking and disturbance rejection capabilities. The system has been tested in simulation using MATLAB/SIMULINK with linear and standard nonlinear load. An experimental setup is implemented to validate the simulation results. The experimental results confirm the satisfactory operation of the SFC with the proposed controller to achieve perfect tracking of 60 Hz reference signals and rejecting 3rd, 5th and 7th harmonics successfully. Eventually, Total Harmonic Distortion (THD) under nonlinear loads is reduced to meet the international standards.

Keywords: Static frequency converter, Shore to ship connection, Resonant controller.

1 INTRODUCTION

Maritime transport is considered one of the highly efficient means of transportation due to its low cost and ability to carry massive loads compared to other means of transportation. More than 90% of the world's trade are transported by cargo ships which supports global trade and supply chains [1]. As maritime technology advances and vessels become more sophisticated, the reliance on electrical systems grows exponentially. Hybrid (diesel– electric) ship propulsion is more economic than the traditional diesel–turbine one due to low fuel consumption [2],[3].

Recently, energy and environmental issues have emerged as remarkably pressing concerns, driven by the relentless rise in greenhouse gas emissions, including CO_2 , NO_x , and CH_4 . Today, the shipping industry accounts for approximately 15% of the total global emissions of nitrogen oxides (NO_x). Therefore, the International Maritime Organization (IMO) has implemented restrictions on ship emissions through its regulatory framework under the international convention for the prevention of pollution from ships (MARPOL) [4],[5],[6].

Shore to ship power connections allow ships docked at port to receive electricity from the local power grid instead of running their onboard diesel generators. This reduces fuel consumption, emissions, and noise while the ship is in port. However, the power grid frequency and voltage may not match the frequency and voltage used by the ship's electrical systems. Therefore, frequency converters are very important [7],[8]. In Port Said shipyard, there are four floating docks and several shore side power connections for the vessels of Suez Canal Authority (SCA) such as dredgers and tugs that need 380V, 50Hz supply and for external vessels, up to 25,000 tons, that need repairs. Some of these vessels need 440V, 60Hz shore power supply. Conventionally, these vessels are fed from docks' generators or from their own generators that causes air pollution and noise in the shipyard.

Traditionally, rotary frequency converters (RFC) have been widely used especially for high power vessels but with the high cost and large size [2]. Static Frequency Converters (SFC) are used to convert the shore power supply to the appropriate frequency and voltage for the ship [7]. Different configurations have been presented in literature, the conventional SFC with three-phase diode bridge rectifier in input stage and three-phase inverter in the output stage is shown in Figure 1(a). This suffers from high total harmonic distortion (THD) and low input power factor which are two important issues should be improved to meet international standards IEEE519 and IEC64020-3 [9]. To reduce the THD, 12 and 24 pulse diode rectifier can be used in input stage as shown in Figure 1(b).(c) [7]. However, these topologies increase the switching losses which affects the system efficiency and cannot achieve unity power factor as well as increases the system size and cost. As an alternative, an Active Front End (AFE) SFC is proposed in [10],[11] to guarantee low THD and unity input power factor. It consists of three phase PWM active rectifier in input stage and three-phase Voltage Source Inverter (VSI) in the output stage as shown in Figure 1(d).

Also, multi-level inverters such as three level neutral point clamped (3L-NPC) can be used in output stage for high voltage SFC to reduce THD but it also has higher switching losses, size, and cost [12].

The loads on the ship may be unbalanced or nonlinear loads such as diode rectifiers in power supplies, variablespeed drives, florescent or LED lamps. These loads draw non sinusoidal currents with third, fifth and seventh harmonics which distort the output voltage at the ship connection and increases the THD. Traditionally, active, passive or hybrid filters can be used to reduce the harmonic contents in output voltage. However, the use of filters increases the size, cost, and complexity of the system, and increases power losses, which reduces the overall efficiency [13].

With the development of modern control systems and the emergence of high-speed microprocessors, it has become possible to solve this problem without using additional filters [13]. Various control techniques have been used to control the SFC output voltage. Cascaded control strategy using Proportional Integral (PI) controller in synchronously rotating reference has been widely used as VSI controller [14],[15],[16]. Although this method is simple but in case of suppling unbalanced and nonlinear loads, it needs some modifications such as sequence decomposition and harmonic compensators which increases the system complexity and needs highperformance DSP controllers.

Alternatively, different nonlinear control strategies have been proposed such as deadbeat control [17], sliding mode control [18], repetitive controllers [19,20] and model predictive controllers [21]. However, all these methods have many drawbacks such as variable switching frequency, low stability margin and high computational effort [22].



Figure 1: Frequency converter configurations [7].

In this paper, a simple and efficient multi-loop control system for shore to ship power connection SFC is proposed. Multi Frequency Quasi-resonant (MFQR) harmonic compensator in stationary reference frame is proposed to mitigate voltage distortions resulting from nonlinear loads. The outer voltage controller consists of a fundamental component Proportional Resonant (PR) controller to force the output voltage to track the sinusoidal reference signal with the required magnitude and frequency, and a multi-frequency resonant harmonic compensator (HC) to reject the 3rd, 5th and 7th harmonic components. While PR controller is used in the inner current controller to force the filter capacitor current to track the reference generated from the outer voltage loop.

The idea behind using the filter capacitor current as a feedback signal instead of filter inductor current is to reduce the inverter output impedance to ensure active damping and good performance with nonlinear or step-changing loads [23],[24].

The mathematical model of the three phase SFC is presented, and a detailed design procedure is described. The proposed control system is designed in the stationary reference frame and analyzed in the frequency domain, evaluating its performance in terms of reference tracking and disturbance rejection capabilities. The system has been simulated using MATLAB/SIMULINK and experimentally validated to verify the simulation results.

2 SFC MATHEMATICAL MODEL

Figure 2 shows the shore to ship power connection SFC. It consists of two stages; the input stage is a threephase active front end (AFE) rectifier to ensure fixed dc link voltage and unity input power factor. While the output stage is a three-phase voltage source inverter (VSI) to control the output voltage magnitude and frequency. A three phase Δ /Y transformer is connected between VSI and the ship to achieve galvanic isolation and four wire connection on the ship side. An LC filter is used to filter the output voltage switching frequency.



Fig.3 shows the per phase equivalent circuit of the load side of the three-phase VSI in the stationary reference frame. The dynamic equations of the system are as in (1),(2) and the corresponding block diagram is shown in Fig.4.

$$v_{conv\alpha\beta}(t) - v_{c\alpha\beta}(t) = L_f \frac{di_{Lf\alpha\beta}(t)}{dt} + R_f i_{Lf\alpha\beta}(t)$$
⁽¹⁾

$$v_{c\alpha\beta}(t) = \frac{1}{C_f} \int (i_{Lf\alpha\beta}(t) - i_{load\alpha\beta}(t))dt$$
⁽²⁾

The VSI controller is responsible for regulating the magnitude and frequency of the fundamental component of the output voltage. This can be performed in the synchronously rotating (dq) using PI controller or in the stationary $(\alpha\beta)$ reference frame using PR controllers. In this paper, the PR controller approach is adopted, as it offers a simpler structure and avoids the requirement for complex synchronization methods.



Figure 3: SFC per phase equivalent circuit in $\alpha\beta$ reference frame.



The transfer function from the converter voltage to the output voltage $G_{io}(s)=V_{c\alpha\beta}(s)/V_{conv\alpha\beta}(s)$ and from load current disturbance to output voltage $G_{do}(s)=V_{c\alpha\beta}(s)/I_{load\alpha\beta}(s)$ are as in (3), (4) respectively.

$$G_{io}(s) = \frac{V_{c\alpha\beta}(s)}{V_{c\alpha\beta}(s)} = \frac{1}{L_c C_c S^2 + R_c C_c S + 1}$$
(3)

$$G_{do}(s) = \frac{V_{c\alpha\beta}(s)}{I_{load\alpha\beta}(s)} = \frac{SL_f + R_f}{L_f C_f S^2 + R_f C_f s + 1}$$
(4)

3 SFC CONVENTIONAL CONTROL SYSTEM

Figure 5 shows the SFC conventional control system in the stationary ($\alpha\beta$) reference frame, it consists of two cascaded control loops, an outer voltage control loop and an inner control loop. The outer voltage control loop forces the output capacitor voltage to track the sinusoidal reference signal with the desired frequency (60 Hz) using PR controller. The output of outer voltage loop is fed to the inner current loop to regulate the filter capacitor current; it also uses PR controller to force capacitor current to track the sinusoidal reference. The reason for using filter capacitor current as a feedback signal instead of filter inductor current is the active damping effect which results in better dynamic response.



Figure 5: SFC conventional controller block diagram.

Resonant controllers are usually used to track sinusoidal references with zero steady state error [25],[26]. In this case the outer loop controls the capacitor voltage to track sinusoidal reference signal with the desired magnitude and frequency. The transfer function of the ideal PR controller is:

$$G_{PR}(s) = k_p + \frac{k_r s}{s^2 + \omega_r^2}$$
(5)

Where, k_p , k_r are the proportional and resonant gains respectively and ω_r is the resonant frequency. Ideal PR controllers have a sharp frequency response characteristic; thus, it cannot work probably under frequency deviations such as in nonlinear loads. To avoid this issue, the Quasi-Proportional Resonant (QPR) controller is proposed in [27] with transfer function as:

$$G_{QPR}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_r^2}$$
(6)

Where, ω_c is the controller cut-off frequency. Fig.6 shows the bode diagram of the PR and QPR controllers.



Figure 6: bode diagram of the ideal and quasi-resonant controllers.

According to Fig. 5, the closed loop transfer function from reference to output $G_{closed}(s)$ is:

$$G_{closed}(s) = \frac{G_{QPRv}(s) * G_{inner}(s)}{1 + G_{QPRv}(s) * G_{inner}(s)}$$
(7)

Where $G_{inner}(s)$ is the closed loop transfer function of the inner current loop as in (8).

$$G_{inner}(s) = \frac{G_{QPRi}(s) * G_{io}(s)}{1 + G_{QPRi}(s) * G_{io}(s) * sC_f}$$
(8)

Where $G_{qprv}(s)$ and $G_{qpri}(s)$ are the outer and inner loop resonant controller transfer functions respectively.

Figure 7 shows the bode diagram of the planet transfer function $G_{io}(s)$ and the overall closed loop transfer function $G_{closed}(s) = V_{c\alpha\beta}(s) / V_{c\alpha\beta}^{*}(s)$. It can be shown that, without QPR controllers the system tracks all input signals with frequencies up to 1000 Hz while, with QPR controllers the system tracks only the 60 Hz reference signals. Besides, the capacitor current feedback active damping technique reduces the high resonant peak at the resonant frequency (1000 Hz) which can affect the system stability.



Regarding the load disturbance rejection capability,

Fig. 8 shows the block diagram from disturbance to output. The transfer function $G_{dist}(s)$ can be derived as:

$$G_{dist}(s) = \frac{V_{c\alpha\beta}(s)}{I_{load\alpha\beta}(s)} = \frac{-\overline{sC_f}}{1 - \frac{G_{FB}(s)}{sC_f(sL_f + R_f)}}$$
(9)

Where $G_{FB}(s)$ is the feedback loop transfer function (10).

$$G_{FB}(s) = -\left[1 + G_{QPRi}(s)\left[G_{QPR\nu}(s) + sC_f\right]\right]$$
(10)



Figure 8: block diagram from disturbance to output.

Fig. 9 shows the bode diagram of the disturbance to output transfer function with and without the QPR $(G_{do}(s), G_{dist}(s))$ respectively. It can be shown that, with QPR the system can reject the 60 Hz disturbances successfully.



4 DESIGN OF THE PROPOSED HARMONIC COMPENSATOR

Regarding, the voltage harmonic compensation, multifrequency resonant terms are added to the fundamental QPR controller to reject these harmonics, the transfer function of the proposed controller is in (11). Where, *h* is the harmonic order (*h*=3,5,7) and k_{rh} and ω_{rh} are the resonant gain and the resonant frequency for the h^{th} harmonic.

$$G_{HC}(s) = \sum_{h=3}^{7} \frac{2k_{rh}\omega_c s}{s^2 + 2\omega_c s + \omega_{rh}^2}$$
(11)

Fig.10 shows the SFC controller with the proposed MFQR-HC in red color. While Fig.11 shows the bode diagram of the open loop and closed loop transfer functions with and without HC ($G_{io}(s)$, $G_{closed}(s)$ and $G_{closed-HC}(s)$) respectively. Besides, Fig.12 shows the bode diagram of the corresponding disturbance to output transfer functions with and without HC ($G_{do}(s)$, $G_{dist}(s)$ and $G_{dist-HC}(s)$) respectively. The QPR controller tracks only the fundamental component in the refence signal and rejects only the disturbances with the fundamental component frequency. While MFQR tracks reference signals with 3rd, 5th and 7th harmonics and rejects the disturbances with these harmonics successfully.



Figure 10: SFC controller with the proposed MFQR HC.

5 SIMULATION RESULTS

The system is simulated in MATLAB/SIMULINK with the parameters listed in Table 1. A standard nonlinear load described by IEC 62040 standard [5] is used for testing. It consists of three-phase bridge rectifier as shown in Fig.13.



Figure 11: bode diagram of $G_{io}(s)$, $G_{closed}(s)$ and $G_{closed-HC}(s)$.



Figure 12: bode diagram of G_{do}(s), G_{dist}(s) and G_{dist-HC}(s).

Table 1. Simulation parameters

parameters	value
Power rating	100kVA
Input voltage and frequency	380V, 50Hz
Output voltage and frequency	440V, 60Hz
DC link voltage	1kV
DC link capacitor	3300µF
Filter capacitor	60µF
Filter inductor	0.41 mH
Switching frequency	5940Hz
Inner current controller parameters	0.7728,
(k_{pi}, k_{ri}, w_c)	188.5,
	1 rad/sec
Outer voltage controller parameters	1,
(k_{pv}, k_{rv}, w_c)	70,
	1 rad/sec
HC parameters (k_{rh}, w_c)	30, 1 rad/sec
Balanced resistive load	3*10Ω
Nonlinear load Rs1, R1, C1	0.077Ω,
	3.5Ω,
	0.35mF



Figure 13: IEC 62040 standard nonlinear load [5].

Fig.14(a),(b) show the load currents and output voltages with balanced resistive load respectively. While Fig.15 (a),(b) show the SFC outer and inner controllers response respectively. The SFC controllers track their sinusoidal references in $\alpha\beta$ correctly. Fig.16(a),(b) show load voltages and currents when supplying the standard nonlinear load described in [5]. The load voltages contain 3rd, 5th and 7th harmonic components due to the distorted load currents and the conventional controller cannot compensate these harmonics. Fig. 16(c) shows that the output voltages harmonics are rejected using the proposed HC. Figs.17,18 show the outer voltage and inner current controllers' in $\alpha\beta$ reference frame response without and with the proposed HC respectively. Without adding the proposed MFQR-HC, they cannot track their references. While, adding 3rd, 5th and 7th resonant terms forces the output voltages and the capacitor currents to track their references with zero steady state error. Finally, Fig.19 shows the corresponding FFT results for the load voltage with and without the proposed MFQR-HC respectively. MFQR-HC reduces the magnitudes of the 3rd,5th and 7th harmonics in load voltages from (2.96%, 8.29% and 1.75%) to (0.39%, 1.08% and 0.92%) respectively and the THD is reduced from 9.39% to 3.05% successfully.







Figure 15: SFC controller responses with normal balanced load $(3*10\Omega)$ (a) outer voltage controller response and (b) inner controller. response.



Figure 16: load voltages and currents with and without the proposed HC (nonlinear load [5]) (a) load currents, (b) output voltages without HC and (c) output voltages with HC.



Figure 17: SFC controller responses (nonlinear load [5]) (without HC) (a) outer voltage controller response and (b) inner controller response.



Figure 18: SFC controller responses (nonlinear load [5]) (with HC) (a) outer voltage controller response and (b) inner controller response.



6 EXPERIMENTAL RESULTS

The proposed SFC is implemented experimentally as shown in Fig. 20 The system block diagram is shown in Fig. 21 The TMS320F28335 DSP controller is used to generate the control signals. IGBT drivers are used to generate PWM signals for the six IGBT switches with 540ns dead time between upper and lower switches. The voltage and current control loops are implemented in MATLAB/SIMULINK using real time simulation toolboxes as shown in Fig. 22. The feedback signals for voltages and currents are obtained using LEM hall sensors.

Figs.23,24 show the load voltages waveforms without and with the proposed HC and the corresponding FFT results are shown in Fig. 25(a), (b). It is obvious that the experimental results agree with the simulation results, and the proposed HC can reduce the 3^{rd} , 5^{th} and 7^{th} harmonic significantly and the THD of output voltages is reduced from 42.79% to 26.56% successfully.

Regarding the outer voltage and inner current controller responses, the experimental results agree with the simulation results as shown in Figs. 26,27 respectively. The SFC proposed controller tracks the voltage and current references successfully.



Figure 20: Experimental setup.



Figure 21: Experimental setup block diagram.



Figure 22: The proposed VSI controller implemented in the Texas Instrument's TMS320F28335 DSP controller.



Figure 23: load voltage waveforms without HC.



Figure 24: load voltage waveforms with HC.



Figure 25: FFT of load voltages with and without the proposed HC (experimental).



Figure 26: outer voltage controller response in $\alpha\beta$ ref. frame with the proposed HC (experimental).



Figure 27: inner current controller response in $\alpha\beta$ ref. frame with the proposed HC (experimental).

7 CONCLUSIONS

Shore to ship power connection is considered one of the basic requirements of maritime ports infrastructure. They equipped with static frequency converters (SFC) to convert the incoming supply frequency to be suitable for the ships at berth.

Nonlinear loads on ships present a critical challenge when designing the shore to ship connections due to their harmful effects such as: increased heating in generators, transformers, and cables due to harmonic currents, malfunction of sensitive electronic equipment due to voltage distortion, and resonance issues that can amplify harmonic voltages and currents. Active or passive filters are usually used to mitigate the effects of nonlinear loads, but they increase the size and cost of the system.

This paper presents a multi-frequency harmonic compensator to solve this problem. In this control scheme, multi-frequency quasi-resonant controller is added to the fundamental frequency controller in the stationary $\alpha\beta$ reference frame to reject the 3rd, 5th and 7th harmonic disturbances in output voltage. The SFC mathematical model and the corresponding transfer functions from reference to output and from disturbance to output are presented.

The system has been simulated in MATLAB/Simulink and tested using normal and standard nonlinear load. The

simulation results have been validated experimentally using TMS320F28335 DSP controller. It can be concluded that the output voltage harmonics can be reduced by 86% and the THD is also reduced by 67.5% using the proposed HC.

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